I claim:

1. A circuit element comprising:

two or more logically entangled bi-directional terminals, wherein each bi-directional terminal can assume any one of three logical states, which are:

(a) a logical true state;

(b) a logical false state; and

(c) an indefinite state, in which state the bi-directional terminal accepts one of the logical true and logical false states as an external input from an external source; and

an entanglement logic for resolving the logical state of each of the bi-directional terminals according to a predetermined set of logical entanglement rules between the bi-directional terminals.

2. A circuit element according to claim 1, wherein the entanglement logic is operable to perform said resolving in response to the external input from the external source.

3. A circuit element according to claim 1, wherein the circuit element comprises several sets of logical entanglement rules and a set of additional terminals, each additional terminal accepting a logical true state or logical false state as an input, wherein the inputs to the set of additional terminals collectively determine which of several sets of logical entanglement rules are to be used for said resolving.

4. A circuit element according to claim 1, wherein the inputs to the set of additional terminals collectively determine the logical state of one or more of the bi-directional terminals.

5. A circuit element according to claim 1, further comprising one or more circuit components, each of which has a high-impedance state, for implementing said indefinite state.

6. A network for logical deduction, the network comprising:

two or more circuit elements, each of which comprises:

two or more logically entangled bi-directional terminals, wherein each bi-directional terminal can assume any one of three logical states, which are:

(a) a logical true state;

(b) a logical false state; and

(c) an indefinite state, in which state the bi-directional terminal accepts one of the logical true and logical false states as an external input from an external source; and

an entanglement logic for resolving the logical state of each of the bi-directional terminals according to a predetermined set of logical entanglement rules between the bi-directional terminals;

wherein the network further comprises a set of additional terminals, each additional terminal accepting a logical true state or logical false state as an input, wherein the inputs to the set of additional terminals collectively determine which of several sets of logical entanglement rules are to be used for said resolving.

7. A network according to claim 6, further comprising an operational coupling of each of several bi-directional terminals of one or more logic elements to one or more additional terminals of another circuit terminal.

8. A network according to claim 7, wherein said operational coupling is modifiable by external input.

9. A network according to claim 6, wherein each of several bi-directional terminals of one or more logic elements is operationally coupled to one or more bi-directional terminals of another circuit terminal.

10. A network according to claim 6, further comprising an interface to a data processing system for controlling and accessing some or all of the bi-directional terminals.

11. A network according to claim 6, wherein the entanglement circuitry comprises bias elements for biasing one or more of the nodes of the network towards one of the logical states, wherein each bias element is weak enough to be overridden by one of the logic elements.

12. A network according to claim 11, wherein the bias elements are responsive to external input from a data processing system.

13. A network according to claim 11, further comprising a data processing system for entering random or pseudorandom values to the bias ele-

ments.

14. A network according to claim 11, further comprising a data processing system that comprises:

a first routine for entering a set of bias values to the bias elements;

a second routine for verifying an output provided by the network under the set of bias values; and

a third routine for modifying the set of bias values and for re-executing the first and second routines until the second routine positively verifies the output.

15. A computer program product including program instructions, wherein the program instructions cause a computer to simulate the circuit element according to claim 1, when said computer program product is run on said computer.

16. A computer program product including program instructions, wherein the program instructions cause a computer to simulate the network according to claim 6, when said computer program product is run on said computer.